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Behavioral Modeling and Analysis of Ground Current in Medium-Voltage Inductors

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***Abstract*- This letter proposes a behavioral model for analyzing the ground current in medium-voltage (MV) inductors. The impedance between the terminals and the ground connection of inductors is measured by the impedance analyzer, which is capacitive at low frequency. In order to characterize this impedance, a multi-stage paralleled RLC circuit is proposed. An analytical method is further developed to calculate parameters of the proposed equivalent circuit, which enables to predict the time-domain response of the ground current in MV inductors. A digital-twin of the double-pulse-test setup is developed in LTspice, where the simulated ground currents show good agreements with the experimental measurements.**

I. Introduction

Medium-voltage (MV) SiC MOSFETs contribute to a significant reduction of switching losses in power modules [1], [2]. However, their fast switching behaviors can introduce high-frequency current oscillations due to the parasitic capacitive couplings from both active and passive components [3]. This poses much challenge to the design of MV filter inductors, whose parasitic capacitive couplings become more significant than other components due to the high inductance resulted from more turns [4]. The common-mode current (ground current) is observed in an MV transformer [5], which has a similar structure to the MV inductor.

It is, therefore, of interest to precisely model and predicts the ground current of MV inductors, which in theory, is determined by both the rate of voltage switching transitions (dv/dt) and the parasitic terminal-to-core couplings together. Both physics-based and behavioral modeling methods can be used to characterize the couplings.

The traditional physics-based modeling methods for calculating the parasitic capacitances of inductors, which can provide physical equations by using geometrical and material information [6], are only valid in the low-frequency range [7], and they usually neglect the modeling of inductance and damping resistance, which are, however, crucial for the behaviors of current oscillations. Besides, the core of the inductor is usually assumed to be floating [6]-[8], where the couplings between the terminals and core are not thoroughly investigated. For high-power MV applications, the core of inductors is usually grounded due to safety considerations. It is indicated that the grounding of inductors will increase the dynamical capacitance of inductor [8], however, the detailed analysis and modeling are still missing.

Therefore, behavioral models, which are basically based on the impedance or voltage/current measurements, are widely used in system-level simulations [9]. The terminals-to-ground coupling is usually modeled as a single capacitor [5], which is only valid before the first resonant frequency. By developing the equivalent circuit models, the behaviors of rotating electrical machines can be characterized using the measured impedance [10], where the valid frequency range can beyond the first resonant point. The chokes, which can be considered as a special type of inductors, are behaviorally modeled by using multiple-stage RLC circuits in series [11]. This allows for characterizing multiple resonant points and valid up to an even higher frequency. However, [11] is not adaptable to characterize the impedance between the terminals and core of MV inductors, where the couplings in between are mainly capacitive.

Thus, this letter will first introduce the ground current in the researched MV inductor, which is caused by the capacitive couplings between the terminal and the ground connection of the inductor. Then, a behavioral model for characterizing these terminal-to-ground couplings is proposed, where the capacitive couplings are represented by a calculated multi-stage paralleled equivalent circuit. An analytical modeling method is proposed to calculate the parameters of the multi-stage paralleled equivalent circuit. The calculated circuit is interfaced to the self-developed LTspice model of the power module [12], where a digital twin of the experimental MV double-pulse-test setup is developed. The simulated ground currents show good agreements with the experimental measurements. Three methods for reducing the ground current in MV filter inductors are given in this letter. The sensitivity analysis of the simulated ground current is presented at the end of this paper.

II. Ground Current in MV Inductors

A medium-voltage double-pulse-test setup is shown in Fig. 1(a). The configuration is enabled by a custom-packaged 10 kV/ 20 A half-bridge SiC MOSFETs power module. A 30 mH 4.16 kV/8 A (RMS) inductor with two U-type amorphous cores is selected as the researched inductor. The inductor is designed with dual windings, and each winding has three layers, with 378 turns in total. The length, width, and height of the researched inductor are 16.5 cm, 12 cm, and 27 cm, respectively.

Fig. 1(b) is the schematic of a medium-voltage double-pulse-test setup with a grounded inductor, where the inductor acts as an inductive load.

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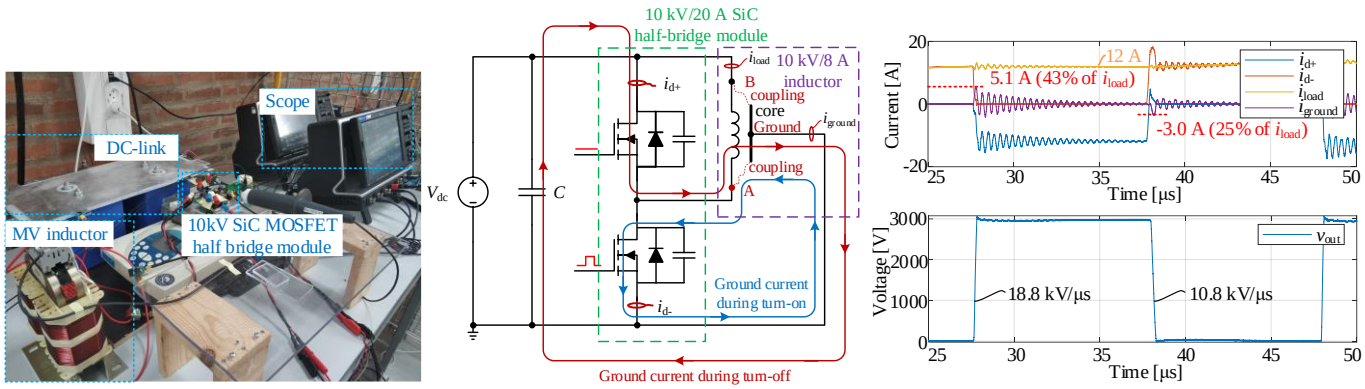

(a) (b) (c)

Fig. 1 Medium-voltage double-pulse test setup. a) Hardware picture. b) Schematic and ground current paths during switch transitions. c) Measured current as well as voltage waveforms of the double-pulse-test.

Due to the high dv/dt at the output of the power module during switching transitions, the ground current of the MV inductor is induced, which circulates in the circuit. The measurement devices used in the setup are listed in Table I.

The paths of the ground current during the turn-on and turn-off switching transitions are highlighted in blue and red, respectively, in Fig. 1(b). A, B, and ground illustrated in Fig. 1(b) are three terminals of the researched inductor, which are also illustrated in Fig. 2(a). In the double-pulse-test, the period of the lower switch is configurated as 115 μs during the first turn-on, where the period of the lower switch is configurated as 10 μs during the second turn-off.

The couplings between terminals and ground contribute to the ground current of MV inductor during switching transitions. Since the terminal B of the inductor is clamped to the DC link, only the coupling between terminal A and ground contributes to the ground current in this case. i_{d+} and i_{d-} are the currents measured at the dc+ and dc- terminal of the half-bridge module, respectively. i_{load} is the load current, and i_{ground} is the ground current.

Table I Measurement devices used in the double-pulse-test setup

	Devices	Maximum bandwidth
i_{d+}, i_{d-}, i_{load}	Pearson 2878 [13]	70 MHz
i_{ground}	Pearson 2877 [14]	200 MHz
v_{out}	Lecroy PPE 20 kV [15]	100 MHz
Oscilloscope	Lecroy HRO64zi [16]	400 MHz

The measured current and voltage of the double-pulse-test are presented in Fig. 1(c). Both ground current and drain current have huge oscillations (43% of load current), which can cause EMI/EMC issues, increase switching losses, and accelerate the aging of the power modules [17].

III. Behavioral Modeling with Equivalent Circuits

The Keysight E4990 impedance analyzer and its adapter 16047 are used for measuring the impedance of the MV inductor. With using the guarding technology [18], the impedance Z_{AG} between the terminal A and ground is measured as a branch of the three-terminal circuit. Fig. 2 is the measured impedance Z_{AG} between the terminal A and ground point, which is capacitive at low frequency and has multiple resonant points above 1 MHz. f_0, f_{A1}-f_{A3}, and f_{R1}-f_{R3} are the selected frequencies for the following model derivations. The valid frequency range of this case is up to 12.85 MHz based on the selected resonant points, where the current harmonics up to 10 MHz are the targets for predicting in this case.

Another method for determining the fitted frequency range is based on the signal to noise ratio of ground current. Although the measurement devices are selected with high bandwidth, it is found that the measured current harmonics will be hidden by the background noise current due to a low signal-to-noise ratio. Therefore, the magnitude of the current harmonics can be calculated by checking the measured impedance and voltage spectrum.

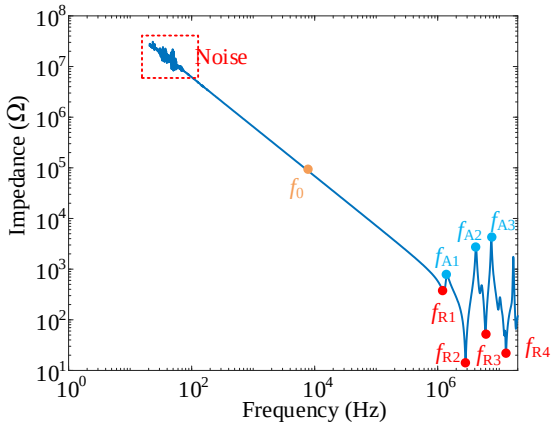

Fig. 2 Measured impedance between the terminal A and ground point of the inductor with selected resonant frequencies.

Fig. 3(a) is a picture of the researched inductor, where Terminal A, Terminal B, and Ground are illustrated. Z_{AG} is dominated by capacitance at low frequency, which is dual to the inductive impedance in [11]. Therefore, a lumped RLC circuit model, which in series first and parallel next, is proposed in Fig. 3(b), which is also dual to the circuit in [11].

Before mathematically deriving the parameters of the equivalent circuit, some assumptions are made:

1) At low-frequency f_0, the impedance is ruled by the capacitance $C_{21} \sim C_{2i}$.
2) A resonance at f_{Ri} is caused by a single series $R_{2i}L_{2i}C_{2i}$ sub-circuit. The influence of other sub-circuits is neglected.

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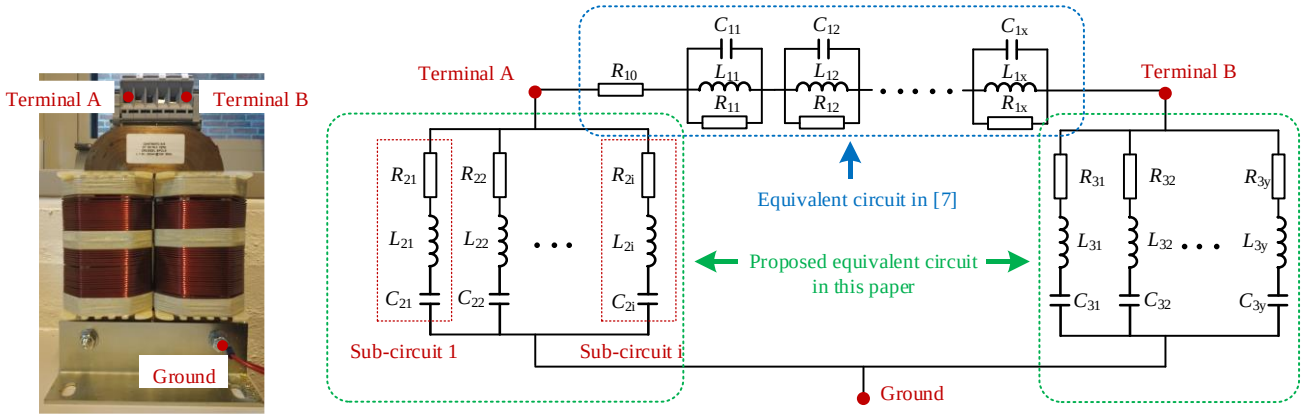

(a) (b)

Fig. 3 MV inductor. a) Photo. b) Equivalent circuit of inductor

Table II Impedance data obtained from measurements

	f_0	f_{R1}	f_{A1}	f_{R2}	f_{A2}	f_{R3}	f_{A3}	f_{R4}
Frequency	4.714 kHz	1.249 MHz	1.432 MHz	2.834 MHz	4.187 MHz	5.948 MHz	7.444 MHz	12.850 MHz
Impedance	143.00 kΩ	347.20 Ω	749.50 Ω	15.80 Ω	2.75 kΩ	51.72 Ω	4.22 kΩ	19.94 Ω

3) An antiresonance at f_{Ai} is caused by the resonance of two sub-circuits $R_{2i}L_{2i}C_{2i}$ and $R_{2i+1}L_{2i+1}C_{2i+1}$. The impact of other sub-circuits is neglected.
4) Some small resonant points are neglected to simplify the calculations and representations of the equivalent *RLC* circuits. For example, a small resonant point between f_{A2} and f_{R3} is neglected in this case.

These assumptions will lead to errors between the measured and fitted impedance. The accuracy of the fitting is even worse if the resonant points are closer.

The number of sub-circuits is equal to the number of selected resonant points. Based on these assumptions, the equation of the impedance at f_0 is derived.

$$\sum_{n=1}^{i} C_{2n} = \frac{1}{2\pi f_0 |Z(f_0)|} \tag{1}$$

Then, L_{2i} is calculated due to the resonance.

$$L_{2i} = \frac{1}{4\pi^2 f_{Ri}^2 C_{2i}} \tag{2}$$

R_{2i} is obtained based on the magnitude of $Z_{R2iL2iC2i}$ at f_{Ri}.

$$R_{2i} = |Z(f_{Ri})| \tag{3}$$

Due to the assumption 4), f_{Ai} is produced by two neighbor sub-circuits, therefore, f_{Ai} is presented as (4).

$$f_{ai} = \frac{1}{2\pi\sqrt{\frac{C_{2i}C_{2i+1}}{C_{2i}+C_{2i+1}}(L_{2i}+L_{2i+1})}} \tag{4}$$

Therefore, C_{2i} can be represented as (5) by simplifying (4).

$$C_{2i+1} = C_{2i}\frac{1-\frac{f_{A1}^2}{f_{Ri+1}^2}}{\frac{f_{A1}^2}{f_{Ri}^2}-1} \tag{5}$$

In this case, four resonant points are selected, therefore an equivalent circuit with four sub-circuits is determined. The magnitude at f_0, f_{R1}-f_{R4}, and f_{A1}-f_{A4} are detected and summarized in Table II. By solving (1)-(5) with the obtained impedance, the parameters of calculated four-stage equivalent circuit is given in Table III. As a comparison, the parameters of a single-stage equivalent circuit which is given by the dominated resonance (f_{R2} in Fig. 2), are listed in Table IV.

Table III Calculated parameters of the four-stage equivalent circuit

	i = 1	i = 2	i = 3	i = 4
R	347.2 Ω	15.8 Ω	51.7 Ω	19.9 Ω
L	382.6 μH	31.4 μH	16.7 μH	3.1 μH
C	42.4 pF	100.5 pF	42.9 pF	50.2 pF

Table IV Calculated parameters of the single-stage equivalent circuit

	R	*L*	*C*
i = 1	13.6 Ω	14.4 μH	223.1 pF

The impedance of the calculated single-stage and four-stage equivalent circuit are compared with the measured impedance in Fig. 4. As expected, the impedance of a four-stage equivalent circuit shows better agreements with the measured impedance than the impedance of the single-stage equivalent circuit.

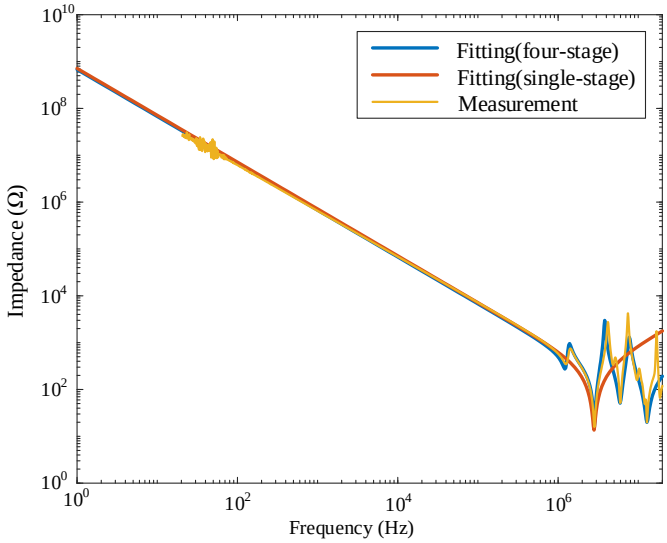

Fig. 4 A comparison between the fitted impedance by using the derived equivalent circuits and the measurement

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IV. Digital-twin Simulations and Experimental Verifications

An LTspice circuit model of the L = 30 mH and 10 kV/20 A SiC MOSFET half-bridge power module is developed [12], where the load current is configured as 12 A during the first turn-on transition. The digital-twin of the tested double-pule-test setup with a grounded inductor is developed in LTspice, where the schematic is presented in Fig. 5. Since the terminal B of the inductor is clamped to the DC link, the impedance network between terminal B and ground is neglected. Since the focus of this paper is the terminal-to-ground network, a simplified equivalent circuit is used between the terminal A and B.

The parasitic parameters of the used double-pulse-test setup are measured by using the Keysight 4990 impedance analyzer and its adapter 16047, which are given in Fig. 5. The simulated ground currents of using the single-stage and four-stage equivalent circuit are compared with the measured ground current in Fig. 6. The ground current of inductor during the first turn-off transition is given in Fig. 6(a), where the ground current during the second turn-on transition is shown in Fig. 6(b).

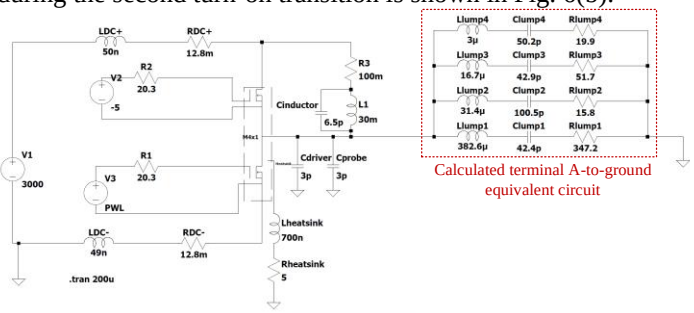
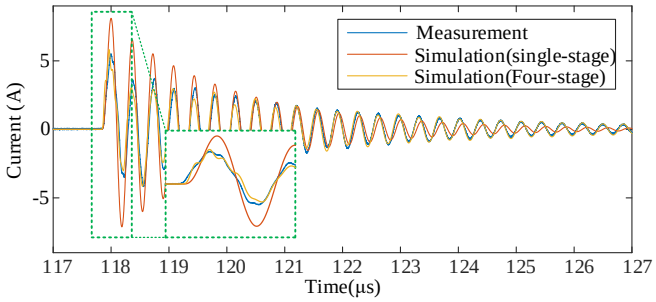


Fig. 5 Circuit simulation of the double-pulse-test with a grounded inductor by using the derived equivalent circuit in LTspice

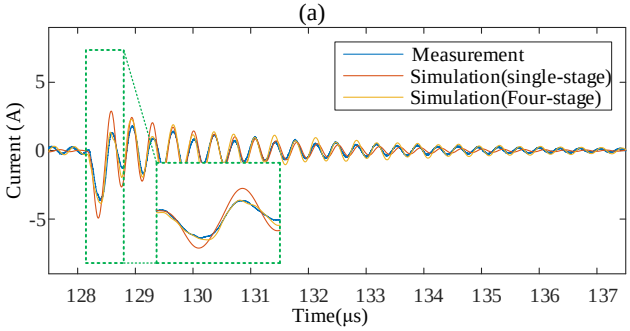
It is found that the digital-twin simulations by using the calculated four-stage equivalent circuit have good agreements with the measured current. In the digital-twin simulations by using the single-stage equivalent circuit, the overshoot currents are 40% and 30% larger than the measured current, which is important in EMI/EMC and switching transient analysis of the system. Besides, the settling time of the digital-twin simulations by using the single-stage equivalent circuit is much shorter than the measured current, and other harmonic currents cannot be found in the zoom-in view of the comparisons.

In order to reduce the ground currents, three methods are suggested as follows:

- Improving the geometrical structures of inductors. The ground current can be reduced if the capacitive couplings between the terminals and ground are weaker.
- Using a damping resistance. A 280 Ω damping resistor is used in series in the ground network of inductors. In Fig. 7, the simulated current during turn-on is used as an example to compare with the measured current, where the overshoot current is reduced by 40%. However, the voltage potential on core and frame is still high during the switching transition due to the damping resistance and transient ground current.
- It is found that the coupling between the terminal at the outer layer and ground is smaller than the coupling between the terminal at the inner layer and ground in inductors with multi-layer structure [20]. Therefore, by connecting the terminal B located at the outer layer of researched MV inductor, can result in 66% overshoot voltage reduction. The simulation has a good agreement with the measurement, which is given in Fig. 8.



(a)



(b)

Fig. 6 Measured and simulated i_{ground} for the first turn-off and second turn-on switching transition by connecting Terminal A to the module

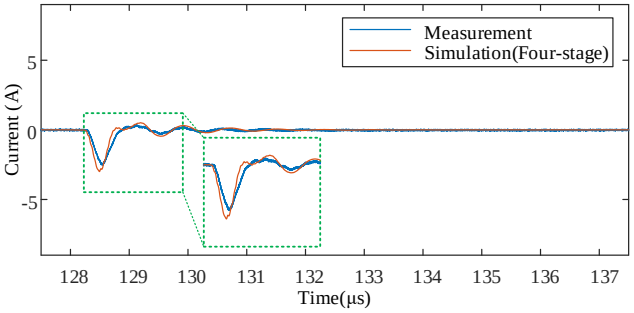


Fig. 7 Measured and simulated i_{ground} for the second turn-on switching transition by using a 280 Ω damping resistor

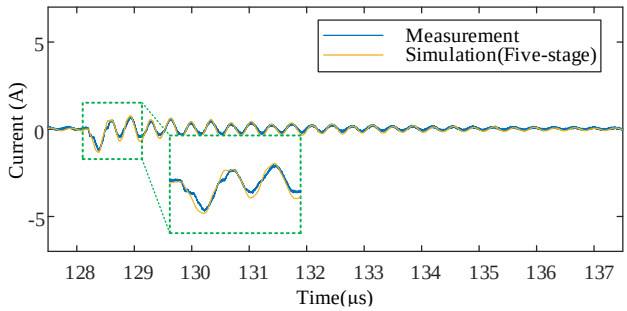


Fig. 8 Measured and simulated i_{ground} for the second turn-on switching transition by connecting Terminal B to the power module

V. Sensitivity Analysis

The simulated ground currents during the first turn-off for four different values of inductance L and circuit parameters are compared with the measured current in Fig. 9.

It is known that the simulated results with a smaller inductance value have a larger load current since the turn-on and turn-off pulse duration for the double pulse is fixed in these

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simulations. Since the dv/dt at turn off increases with higher load current in case of small inductance [19], therefore, the orange curve (L = 27 mH) has the largest overshoot current in Fig. 10, since it has the highest load current in these four cases. Similarly, the purple curve is the simulated ground current with the 30 mH inductor, where L_{DC+}, R_{DC+}, L_{DC-}, R_{DC-}, $L_{heatsink}$, $R_{heatsink}$, C_{probe}, and C_{driver} are removed. Compared to the orange curve (L = 30 mH, with parasitic circuit parameters), the purple curve has a larger overshoot current, where it has less parasitic capacitances in the circuit and therefore, in that case, the dv/dt and v_{out} is higher.

The derived behavioral model is not sensitive to the circuit parameters of the test setup. However, the overshoot voltage of the simulated ground current is sensitive to the parasitic circuit parameters, where the dv/dt at the output voltage can be easily changed by the load current and parasitic circuit parameters. The derived behavioral model can be simulated in conjunction with using the semiconductor circuit models, measured voltage signals, or simply by using a ramp function. By using the voltage excitation with more accurate dv/dt values, the developed behavioral model can predict the ground currents more precisely.

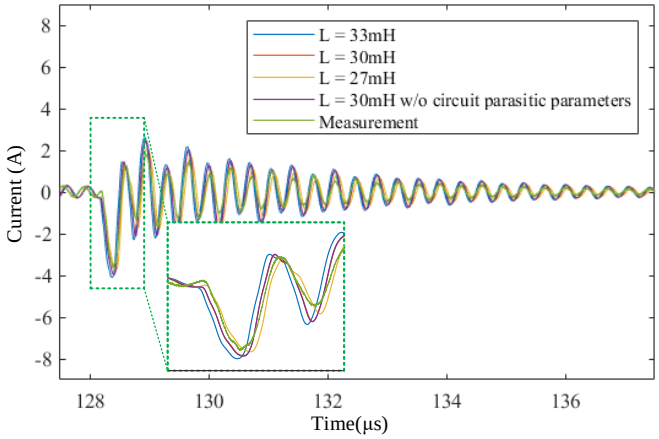

Fig. 9 Comparison of the Simulated and measured ground current of for four different cases and during the first turn-off transition

VI. Conclusions

This letter proposed an analytically behavioral model for characterizing the ground current in MV inductors, where the capacitive impedance between the terminals and core of inductors is represented by a calculated multi-stage paralleled RLC circuit. By using a digital twin of a double-pulse-test setup in LTspice, the ground current is accurately simulated, and three methods for reducing the ground current in MV filter inductors are also presented. The sensitivity analysis of simulated ground current is given. This research show potentials for future system-level digital-twin designs. The proposed model is also modulable and scalable, which is also valid for characterizing the capacitive couplings in other applications.

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